REMARKS

Claims 1-3, 5-9 and 11 have been amended. Claims 12-15 have been added. Claims 1-15 remain for further consideration. The specification has been amended to correct several typographical errors. A drawing amendment is also enclosed. No new matter has been added.

The objections and rejections shall be taken up in the order presented in the Official Action.

1. Claims 1-15 are now pending.

2. A proposed drawing amendment is enclosed herewith. With respect to the objections set forth in the Official Action, the following action has been taken:

- FIGs. 1 and 2 have been labeled as "PRIOR ART".
- FIG. 1 is not a block diagram illustration, and thus does not lend itself to the use of textual descriptions. Textual descriptions have been added to certain figure elements in the block diagram illustrations, as is convention in practice before the Office.
- Again, element 13 does not lend itself to the use of textual descriptions. In addition, it is respectfully submitted that adding textual descriptions is unnecessary, and takes away from a proper understanding of the claimed invention.
- The element number for the data bus has been changed.
- Elements 30, 32, 48, 54 and 56 do not lend itself to the use of textual descriptions and unnecessarily lead to text in the figures that does not provide further assistance in understanding the claimed invention.

If the Examiner elects to maintain the position that textual descriptions should be added to the

figures as set forth in the Official Action, the Examiner is invited to call the undersigned to discuss this matter.

3. The title has been amended.

4. The Abstract has been amended.

5. Claim 5 currently stands objected to. Claim 5 has been amended to now depend from claim 1.

6-7. Claims 1, 5, 9 and 11 currently stand rejected for allegedly being anticipated by Applicant's Admitted Prior Art (hereinafter "AAPA").

Claim 1 recites a circuit arrangement for transferring data between a data transmitter and a plurality of data receivers. The circuit arrangement includes:

> "a buffer device that receives a data signal from the data transmitter and provides a buffered data signal onto a data bus;
> a first memory element configured and arranged a non-sequential component coupled to said data bus to receive and store said buffered signal and provide a first stored signal;
> a plurality of second memory elements that receive and store said first stored signal and each provide an associated second stored signal to its associated one of said plurality of data receivers; and
> a controller that controls the output state of said buffer device, to control the transfer of data from said first memory element to said second memory element." (emphasis added, cl. 1)

AAPA neither discloses nor suggests a circuit arrangement as recited in claim 1 that includes a first memory element configured and arranged a non-sequential component coupled to the data bus. Prior

Art FIG. 2 illustrates a memory device that is controlled by the controller (e.g., clocked) and as a memory device it is clearly not a non-sequential component as recited in claim 1. A 35 U.S.C. §102 rejection requires that a single reference teach each and every element of the claimed invention. Hence, AAPA is incapable of anticipating claim 1.

Claim 11 recites an integrated circuit arrangement for transferring data between a data transmitter and a plurality of data receivers. The integrated circuit arrangement includes:

> "means for receiving a data signal from the data transmitter and for providing a buffered data signal onto a data bus;
> a first non-sequential memory element coupled to said data bus to receive and store said buffered data signal, and provide a first stored signal;
> a plurality of second memory elements that each receives and stores said first stored signal, and provides a second stored signal to its associated one of the plurality of data receivers; and
> a controller that selectively enables the storage of said buffered data signal in said first memory element and the storage of said first stored signal in said plurality of second memory elements." (emphasis added, cl. 11).

As set forth above, AAPA neither discloses nor suggests a first non-sequential memory element coupled to the data bus to receive and store the buffered data signal, and provide a first stored signal. Prior Art FIG. 2 illustrates a memory device that is controlled by the controller (e.g., clocked) and as a memory device it is clearly not a non-sequential component as recited in claim 1. A 35 U.S.C. §102 rejection requires that a single reference teach each and every element of the claimed invention. Hence, AAPA is incapable of anticipating claim 11.

New claim 15 recites an integrated circuit arrangement for transferring data between a data transmitter and a plurality of data receivers also located on the integrated circuit arrangement. The integrated circuit arrangement includes:

> "a receiving circuit for receiving a data signal from the data transmitter and for providing a buffered data signal onto a data bus;
>
> a capacitive element coupled to said data bus to receive and store said buffered data signal, and provide a first stored signal;
>
> a plurality of memory elements that receive and store said first stored signal, and provide a second stored signal to an associated one of said plurality of data receivers; and
>
> a controller that selectively enables the transfer of information into said capacitive element and said memory elements." (emphasis added, cl. 15).

AAPA neither discloses nor suggests a capacitive element coupled to the data bus to operate as set forth in claim 15. For at least this reason AAPA is incapable on anticipating the subject matter set forth in claim 15.

It is alleged in the Official Action that a person of ordinary skill in the art at the time of the present invention would have modified AAPA based upon the teaching of U.S. Patent 4,567,561 to Wyatt (hereinafter "Wyatt") for a number of different reasons (see Official Action, pg. 6). However, there is no suggestion of record that would have allegedly suggested to such a skilled person to replace memory devices uniquely associated with each of the data receives (see FIG. 2, a first memory device is uniquely associated with each data receiver). That is, if the person of ordinary skill was motivated to replace the first memory devices 20 as illustrated in FIG. 2 with parasitic capacitance as suggested, then this one-to-one type replacement would have lead to various parasitic capacitances being arranged in parallel. As known arranging capacitances in parallel causes the capacitances to sum. As a result, such an arrangement of replacing with various first memory devices 20 with parasitic capacitance would lead to an increase in bus capacitance proportional to the number N of data receivers on the IC, and such an increase in capacitance would of course reduce the operating speed of the bus.

In contrast, the claimed invention utilizes a first memory element configured and arranged as

a non-sequential component couple to said data bus to receive and store said buffered signal and provide a first stored signal. The first stored signal is provided to each of the plurality of second memory elements that each provide an associated second stored signal to its associated one of said plurality of data receivers. That is, in the AAPA the each of the first memory devices were parallel to one another, such that there was a dedicated first memory device for each data receiver. In contrast, the claimed invention uses a first memory element that is coupled to the data bus and is not uniquely associated with to any one of the data receivers.

8-9. Claims 2-4, 6 and 10 currently stand rejected for allegedly being obvious in view of AAPA in combination with U.S. Patent 4,567,561 to Wyatt (hereinafter "Wyatt").

It is respectfully submitted that this rejection is now moot since the independent claims from which these claims depend, either directly or indirectly, are patentable for at least the reasons set forth above.

10. Claims 7-8 currently stand rejected for allegedly being obvious in view of AAPA in combination with U.S. Patent 6,378,011 to Moore (hereinafter "Moore") and U.S. Patent 5,293,378 to Shimizu (hereinafter "Shimizu").

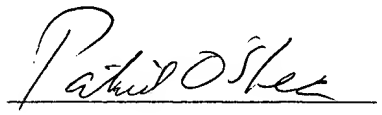
It is respectfully submitted that this rejection is now moot since the independent claims from which these claims depend, either directly or indirectly, are patentable for at least the reasons set forth above.

11. The additional cited prior art is noted, and the undersigned agrees that these references, either alone or in combination, fail to render the claimed invention unpatentable.

For all the foregoing reasons, reconsideration and allowance of claims 1-15 is respectfully requested.

If a telephone interview could assist in the prosecution of this application, please call the undersigned attorney.

Respectfully submitted,



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~~A CIRCUIT ARRANGEMENT WITH A DATA TRANSFER DEVICE~~ APPARATUS USING BUS CAPACITANCE TO PERFORM DATA STORAGE DURING DATA TRANSFER ACROSS THE BUS

BACKGROUND OF THE INVENTION

The present invention relates to a circuit arrangement with two or more circuit components that cooperate through a data transfer device, and in particular to an integrated circuit arrangement for transferring data between a data transmitter and a data receiver.

Circuit arrangements often have a digital and/or an analog/digital integrated circuit, and are generally referred to as mixed-signal ICs. A circuit arrangement with such a structure is illustrated in FIG. 1. The circuit arrangement includes a first circuit section 1, a second circuit section 2 and a data transfer device 3 between the first and second sections.

Referring still to FIG. 1, the first circuit section 1 designates the above-mentioned integrated circuit, which is embedded in the second circuit section 2, and which is connected to this by communication buses or connection lines. The second circuit section 2 can have output or bond pads. Output terminals, which form the interface of the circuit arrangement and thus of the integrated circuit to the outside world may be bonded on these bond pads. However, it would also be conceivable that the second circuit section 2 is also structured as an integrated circuit in which the integrated circuit of the first circuit section 1 is embedded. Circuit arrangements with such a structure are, for example, representatives of integrated circuits technically known as "cell-based systems" or "systems on silicon" or "circuits with embedded macros." With integrated circuits of this kind, the first circuit section 1 (cell or embedded macro) frequently is an already-existing functional block, which is only embedded in a new environment (the second circuit section).

Both the first and second circuit sections 1, 2 typically need a fixed chip surface due to their

functionality or their manufacturing technology, especially in the case of chip bonding, ESD protection, etc. Consequently, the chip surface cannot be further optimized without major interventions in the functionality or technology. However, the chip surface is often largely determined by the data transfer device 3 that is needed between the circuit sections. Particularly in very complex systems (e.g., signal processors, processors, microcontrollers, etc.) this can sometimes be much larger than the integrated circuit itself.

A typical data transfer device 3 is illustrated in FIG. 2. The device includes a data transmitter 10, a data receiver 12, and a data bus 174. The data transmitter 10 sends data via a first data buffer 16 and via the data bus 174 to a plurality N of data receivers 12-15. Each data receiver 12-15 has associated with it a second data buffer 18 and two memory devices 20, 22. The two memory devices 20, 22 associated with the data receiver 12 are arranged in a master-slave structure. During data transfer, this structure allows transfer of the data from the data bus 174 to the data receiver 12. This is made possible by a process controller 24 that opens the first memory device 20 acting as master, and does not close it until this memory device contains updated (i.e., valid) data. At this moment, under the control of the process controller 24, the first memory device 20 is closed, and the second memory device 22, acting as slave, is opened. This ensures that only valid, error-free data are read out on the receiver side.

However, for the data transfer device 3, the surface area needed for two memory devices 20, 22 becomes greater and greater as more receivers are connected to the data bus 174. As a result, and as a result of layout-based contingencies, the region associated with the data transfer device 3 (FIG. 1) often becomes disproportionately large compared to the integrated circuit 1 and the pad region 2. The problem of a double surface expenditure for two memory elements for each receiver consequently is often unacceptable, just for reasons of cost.

Therefore, there is a need for a circuit arrangement whose design optimizes the surface of the data transfer device.

SUMMARY OF THE INVENTION

Briefly, according an aspect of the present invention, a circuit arrangement for transferring data between a data transmitter and a data receiver includes a buffer device that receives a data signal from the data transmitter and provides a buffered data signal onto a data bus. A first memory element receives and stores the buffered signal on the data bus and provides a first stored signal. A second memory element receives and stores the first stored signal and provides a second stored signal to the data receiver. A controller controls the output state of the buffer device, to control the transfer of data between the first and second memory elements.

The invention solves the problem of double surface expenditure for two memory devices for each receiver, in that the data bus itself takes over the role of one of these memory devices (i.e., the memory device which functions as master). A single memory device is integrated onto the data bus and takes over the role of the no longer needed memory device for each data receiver. By saving one of the memory devices associated with each receiver, the integrated circuit surface area associated with the data transfer devices may be optimized, resulting in a reduction of surface area and thus a reduction of cost.

These memory devices may be implemented by capacitances and/or holding elements. In one embodiment, the capacitive element is realized from the capacitance of the data bus lines with respect to one or more reference lines. In this case, the function of the inventive data transfer device is still assured even if no dedicated capacitive component is provided.

The invention is especially suitable for complex integrated circuits, such as for example microprocessors, microcontrollers and signal processors.

These and other objects, features and advantages of the present invention will become apparent in light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING

FIG. 1 is a schematic illustration of a generic circuit arrangement;

FIG. 2 is a schematic illustration of a prior art transfer device that includes a first circuit section acting as data transmitter and at least one second circuit section acting as data receiver;

FIG. 3 illustrates a first embodiment of an inventive data transfer device; and

FIG. 4 illustrates a second embodiment of an inventive data transfer device.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 3 is a schematic illustration of a data transfer device 30 between a first circuit section that includes the data transmitter 10, and at least one second circuit section that includes the data receiver 12a. The data transfer device 30 includes a data bus 32 operably positioned between the data transmitter 10 and the data receiver 12a. On the transmitter side, first data buffer 16 is disposed in the data bus 32~~14~~. The receiver side includes a plurality N of receiver cells $Z_1 ... Z_N$. Each receiver cell $Z_1 ... Z_N$ includes an associated data receiver 12, each of these being preceded by second memory device 22 and second data buffer 18. The data buffers 16, 18 can be controlled and implemented in a well-known manner by inverters. The second memory device 22 can also be controlled, and implemented as a conventional flip-flop, latch, etc.

A process controller 40 controls the data transfer between the data transmitter 10 and the data receiver 12a. For this purpose, the process controller 40 is connected by control lines 42-46 to the data transmitter 10, the data receiver 12a, the data buffers 16, 18, and the second memory device 22.

According to an aspect of the present invention, the data transfer device 30 includes a first memory element 48 coupled to the data bus 32. The first memory element 48 is arranged such that it precedes (i.e., it is upstream of) each receiver cell $Z_1 ... Z_N$, and thus precedes the second memory device 22. In this embodiment, the first memory element 48 is constructed as a capacitive element C 50, which is connected between the data bus 32 and a reference potential 52.

FIG. 4 illustrates a second embodiment of an~~the~~ inventive data transfer device 53~~30~~, that includes a first memory device 54 constructed as a holding element 56 that is connected to the data bus 32. The function of the data transfer devices ~~3~~ shown in FIGs. 3 and 4 will now be discussed in more detail.

Referring to FIGs. 3 and 4, the data transmitter 10 transmits data via the data buffer 16 and the data bus 32. The data are held for a certain time on the data bus 32, either dynamically by the first memory element 48 constructed as a capacitive element C 50 (see FIG. 3), or statically by an additional holding element 56 (see FIG. 4). This holding or storing action takes place because a control signal(s) from the controller ~~40~~ maintains the first data buffer 16 in a high-ohm state (i.e., a high impedance state). Subsequently, a control signal(s) from the controller ~~24~~ opens the second memory device 22 causing the desired valid data that are stored on the data bus 32 to be transferred into the respective second memory device 22. Then the second memory device 22 is again locked. The data bus 32 then can assume arbitrary states (i.e., for example, it can again accept data for the next data transfer).

The capacitive element C 50 in FIG. 3 may be realized by an integrated or a discrete

capacitance. In one embodiment the capacitive element C 50 in FIG. 3 is realized by the capacitance of the data bus lines 32 with respect to one or more reference lines. In this case, the function of the inventive data transfer device is assured even if no dedicated capacitive element C is present. It is only necessary to suitably modify the controller 40, especially the activation of the first data buffer 16 to control the transfer of data to the second memory 22.

Referring to FIG. 4, it may be desirable to sub-divide the controller ~~40~~ into two circuit sections 60, 62, if this provides additional saving of area and/or an increase of operating speed. In this case, which is shown in FIG. 4, a first circuit section 60 of the process controller is assigned to the data transmitter 10, and a second circuit section 62 of the process controller is assigned to each of the data receivers. An additional control bus 64 is located between the process controls 60, 62 to enable communication between the process controls.

The inventive circuit arrangement is applicable to all possible technologies. The invention is especially advantageous if the circuit arrangement is an integrated circuit. However, a discrete realization may also be used over either short or very long distances. In principle, the inventive data transfer device is applicable to all digital, analog, and mixed-signal devices (i.e., analog/digital circuit arrangements). In addition, the invention is not restricted exclusively to electric circuit arrangements, but can also be expanded to pneumatically operating circuit arrangements. In the case of a transfer device in a pneumatic system, the data buffers, for example, are realized as valves, the memory devices as pressurized containers, and the data buses as conventional lines.

An advantage of the invention is that it provides a saving of area and thus material. In addition, the present invention requires only a slight modification of the process control, and the addition of a memory device for all associated receivers, which can be realized with a capacitive element or a simple holding element.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is: